CLAIMS

What is claimed is:

1. A method to modulate address data of a disc type recording medium, the method comprising:

generating the address data;

performing error correction coding of the address data and outputting coded address data;

receiving the coded address data in a unit of at least two bits;

generating a first modulated signal of the coded address data using a first modulation technique;

generating a second modulated signal of the coded address data using a second modulating signal; and

generating a unit wobble signal by synthesizing the first and second modulated signals.

2. The method of claim 1, wherein the generation of the first modulated signal comprises generating a signal using the first modulation technique indicating each bit value of the coded address data and generating the second modulated signal using the second modulation technique by generating a signal indicating each bit value of the coded address data.

3. The method of claim 1, wherein the generation of the first modulated signal comprises, using the first modulation technique, generating a predetermined pattern signal if a bit value of the coded address data is equal to a first bit value and not generating the predetermined pattern signal if the bit value of the coded address data is equal to a second bit value, and generating the second modulated signal using the second modulation technique by generating the signal indicating each bit value of the coded address data.

4. The method of claim 1, wherein the generation of the first modulated signal comprises generating a signal using the first modulation technique to distinguish signals indicating each bit value from one another, and generating the second modulated signal using the second modulation technique by generating signals having different lengths for each at least two-bit values of coded address data.

5. The method of claim 1, wherein the generation of the first modulated signal comprises generating at least two pattern signals indicating at least two-bit values of the coded address data using the first modulation technique, and generating the second modulated signal using the first modulation technique by generating at least two signals used to distinguish signals indicating a bit value of the address data using the second modulation technique, where the coded address data of at least two bits is indicated by disposing at least two pattern signals in predetermined locations and inserting at least two signals to distinguish signals indicating a bit value of the address data between the at least two pattern signals.

6. The method of claim 2, wherein the generation of the unit wobble signal comprises disposing the first and second modulated signals adjacent to each other.

7. The method of claim 2, wherein the generation of the unit wobble signal comprises alternating the first and second modulated signals.

8. The method of claim 4, further comprising:

generating signals indicating each bit of the coded address data.

9. The method of claim 2, further comprising:

generating a signal indicating a start of the coded address data using one of the first and second modulation techniques and a third modulation technique.

10. The method of claim 3, further comprising:

generating a signal indicating a start of the coded address data using one of the first and second modulation techniques and a third modulation technique.

11. The method of claim 4, further comprising:

generating a signal indicating a start of the coded address data using one of the first and second modulation techniques and a third modulation technique.

12. The method of claim 5, further comprising:

generating a signal indicating a start of the coded address data using one of the first and second modulation techniques and a third modulation technique.

13. The method of claim 2, wherein the first modulation technique is binary phase shift keying (BPSK), and the second modulation technique is frequency shift keying (FSK).

14. The method of claim 3, wherein the first modulation technique is binary phase shift keying (BPSK), and the second modulation technique is frequency shift keying (FSK).

15. The method of claim 4, wherein the first modulation technique is binary phase shift keying (BPSK), and the second modulation technique is frequency shift keying (FSK).

16. The method of claim 5, wherein the first modulation technique is binary phase shift keying (BPSK), and the second modulation technique is frequency shift keying (FSK).

17. An apparatus to modulate address data of a disc-type recording medium, the apparatus comprising:

an address data generating unit generating the address data;

an error correction coding unit performing error correction coding of the address data received from the address data generating unit and outputting coded address data;

a modulating unit generating a first modulated signal of the coded address using a first modulation technique and a second modulated signal of the coded address using a second modulation technique, after receiving the coded address data in a unit of at least two bits from the error correction coding unit; and

a wobble signal generating unit generating a unit wobble signal by synthesizing the first and second modulated signals received from the modulating unit.

18. The apparatus of claim 17, wherein the modulating unit comprises:

a first modulator generating the first modulated signal using the first modulation technique by generating signals indicating each bit value of the coded address data; and

a second modulator generating the second modulated signal using the second modulation technique by generating signals indicating each bit value of the coded address data.

19. The apparatus of claim 17, wherein the modulating unit comprises:

a first modulator generating the first modulated signal using the first modulation technique by generating a predetermined pattern signal if a bit value of the coded address data is equal to a first bit value and not generating the predetermined pattern signal if the bit value of the coded address data is equal to a second bit value; and

a second modulator generating the second modulated signal using the second modulation technique by generating a signal indicating each bit value of the coded address data.

20. The apparatus of claim 17, wherein the modulating unit further comprises:

a first modulator generating the first modulated signal using the first modulation technique by generating a signal used to distinguish signals indicating a bit value of the address data; and

a second modulator generating the second modulated signal using the second modulation technique by generating signals with different lengths indicating each at least two-bit values of the coded address data.

21. The apparatus of claim 17, wherein the modulating unit further comprises:

a first modulator generating the first modulated signal using the first modulation technique by generating at least two pattern signals indicating at least two-bit values of the coded address data; and

a second modulator generating the second modulated signal using the second modulation technique by generating at least two signals to distinguish signals indicating a bit value of the address data,

wherein, the coded address data of at least two bits is indicated by disposing at least two pattern signals in predetermined locations and inserting the at least two signals to distinguish the signals indicating a bit value of the address data between the at least two pattern signals.

22. The apparatus of claim 18, wherein the wobble signal generating unit generates the unit wobble signal by disposing the first and second modulated signals adjacent to each other.

23. The apparatus of claim 18, wherein the wobble signal generating unit generates the unit wobble signal by alternating the first and second modulated signals.

24. The apparatus of claim 20, wherein the second modulator generates signals indicating each bit of the coded address data.

25. The apparatus of claim 18, wherein the first modulator generates a signal indicating a start of the coded address data using one of the first and second modulation techniques and a third modulation technique.

26. The apparatus of claim 19, wherein the first modulator generates a signal indicating a start of the coded address data using one of the first and second modulation techniques and a third modulation technique.

27. The apparatus of claim 20, wherein the first modulator generates a signal indicating a start of the coded address data using one of the first and second modulation techniques and a third modulation technique.

28. The apparatus of claim 21, wherein the first modulator generates a signal indicating a start of the coded address data using one of the first and second modulation techniques and a third modulation technique.

29. The apparatus of claim 18, wherein the first modulation technique is a binary phase shift keying (BPSK) and the second modulation technique is a frequency shift keying (FSK).

30. The apparatus of claim 19, wherein the first modulation technique is a binary phase shift keying (BPSK) and the second modulation technique is a frequency shift keying (FSK).

31. The apparatus of claim 20, wherein the first modulation technique is a binary phase shift keying (BPSK) and the second modulation technique is a frequency shift keying (FSK).

32. The apparatus of claim 21, wherein the first modulation technique is a binary phase shift keying (BPSK) and the second modulation technique is a frequency shift keying (FSK).

33. A method to demodulate address data of a disc type recording medium, the method comprising:

after receiving a unit wobble signal indicating the address data of at least two bits, which is generated by a synthesizing signal modulated by using first and second modulation techniques, demodulating using the first demodulation technique the signal modulated by the first modulation technique into data of the at least two bits, and demodulating using the second demodulation technique the signal modulated using the second modulation technique into the data of the at least two bits;

determining the address data based on the data demodulated by using the first and second demodulation techniques;

if values of the data of the at least two bits demodulated by using the first and second demodulation techniques are different from each other, generating an eraser flag signal indicating mismatched bit positions; and

outputting the address data after performing error correction decoding on the address data and after generating the eraser flag signal.

34. The method of claim 33, further comprising:

performing the demodulation using the first demodulation technique of the signal modulated by using the first modulation technique into a first bit value of the address data, if a predetermined pattern signal exists;

demodulating using the second demodulation technique, the signal modulated by using the first modulation technique into a second bit value of the address data, if the predetermined pattern signal does not exist; and

demodulating using the second demodulation technique each bit value of the signal modulated by using the second modulation technique.

35. The method of claim 33, wherein the first demodulation technique is a binary phase shift keying (BPSK) and the second demodulation technique is a frequency shift keying (FSK).

36. The method of claim 34, wherein the first demodulation technique is a binary phase shift keying (BPSK) and the second demodulation technique is a frequency shift keying (FSK).

37. An apparatus to demodulate address data of a disc type recording medium, the apparatus comprising:

a demodulating unit, after receiving a unit wobble signal indicating the address data of at least two bits generated by synthesizing signals modulated by first and second modulation techniques, demodulating using the first demodulation technique, the signal modulated by using the first modulation technique into data of the at least two bits, and demodulating using the second demodulation technique the signal modulated by using the second modulation technique into data of the at least two bits;

a data determining unit determining the address data based on the data demodulated by using the first and second demodulation techniques and generates an eraser flag signal indicating mismatched bit positions if values of the data demodulated by using the first and second demodulation techniques are different from each other; and

an error correction decoding unit performing error correction decoding of the determined address data and the eraser flag signal.

38. The apparatus of claim 37, the demodulating unit comprises:

a first demodulator demodulating the data using the first demodulation technique; and

a second demodulator demodulating the data using the second demodulation technique.

39. The apparatus of claim 37, wherein the demodulating unit comprises:

a first demodulator demodulating, using the first demodulation technique, the signal modulated by using the first modulation technique into a first bit value of the address data, if a predetermined pattern signal exists, and demodulating, using the first demodulation technique, the signal modulated by using the first modulation technique into a second bit value of the address data if the predetermined pattern signal does not exist; and

a second demodulator demodulating, using the second demodulation technique, each bit value of the signal modulated by using the second modulation technique.

40. The apparatus of claim 37, wherein the first demodulation technique is a binary phase shift keying (BPSK) and the second demodulation technique is a frequency shift keying (FSK).

41. The apparatus of claim 38, wherein the first demodulation technique is a binary phase shift keying (BPSK) and the second demodulation technique is a frequency shift keying (FSK).

42. The apparatus of claim 39, wherein the first demodulation technique is a binary phase shift keying (BPSK) and the second demodulation technique is a frequency shift keying (FSK).

43. A computer readable storage medium controlling a computer and having recorded thereon address data modulated by a process of:

generating the address data;

performing error correction coding of the address data and outputting coded address data;

receiving the coded address data in a unit of at least two bits;

generating a first modulated signal of the coded address data using a first modulation technique;

generating a second modulated signal of the coded address data using a second modulating signal; and

generating a unit wobble signal by synthesizing the first and second modulated signals.

44. The computer readable storage medium of claim 43, wherein the generation of the first modulated signal comprises generating a signal using the first modulation technique indicating each bit value of the coded address data and generating the second modulated signal using the second modulation technique by generating a signal indicating each bit value of the coded address data.

45. The computer readable storage medium of claim 43, wherein the generation of the first modulated signal comprises, using the first modulation technique, generating a predetermined pattern signal if a bit value of the coded address data is equal to a first bit value and not generating the predetermined pattern signal if the bit value of the coded address data is equal to a second bit value, and generating the second modulated signal using the second modulation technique by generating the signal indicating each bit value of the coded address data.

46. The computer readable storage medium of claim 43, wherein the generation of the first modulated signal comprises generating a signal using the first modulation technique to distinguish signals indicating each bit value from one another, and generating the second modulated signal using the second modulation technique by generating signals having different lengths for each at least two-bit values of coded address data.

47. The computer readable storage medium of claim 43, wherein the generation of the first modulated signal comprises generating at least two pattern signals indicating at least two-bit values of the coded address data using the first modulation technique, and generating the second modulated signal using the first modulation technique by generating at least two signals used to distinguish signals indicating a bit value of the address data using the second modulation technique, where the coded address data of at least two bits is indicated by disposing at least two pattern signals in predetermined locations and inserting at least two signals to distinguish signals indicating a bit value of the address data between at least two pattern signals.

48. The computer readable storage medium of claim 44, wherein the generation of the unit wobble signal comprises disposing the first and second modulated signals adjacent to each other.

49. The computer readable storage medium of claim 44, wherein the generation of the unit wobble signal comprises alternating the first and second modulated signals.

50. The computer readable storage medium of claim 46, further comprising:
generating signals indicating each bit of the coded address data.

51. A computer readable storage medium controlling a computer and comprising a process of:

generating the address data;

performing error correction coding of the address data and outputting coded address data;

receiving the coded address data in a unit of at least two bits;

generating a first modulated signal of the coded address data using a first modulation technique;

generating a second modulated signal of the coded address data using a second modulating signal; and

generating a unit wobble signal by synthesizing the first and second modulated signals.

52. The computer readable storage medium of claim 51, wherein the generation of the first modulated signal comprises generating a signal using the first modulation technique indicating each bit value of the coded address data and generating the second modulated signal using the second modulation technique by generating a signal indicating each bit value of the coded address data.

53. The computer readable storage medium of claim 51, wherein the generation of the first modulated signal comprises, using the first modulation technique, generating a predetermined pattern signal if a bit value of the coded address data is equal to a first bit value and not generating the predetermined pattern signal if the bit value of the coded address data is equal to a second bit value, and generating the second modulated signal using the second modulation technique by generating the signal indicating each bit value of the coded address data.

54. The computer readable storage medium of claim 51, wherein the generation of the first modulated signal comprises generating a signal using the first modulation technique to distinguish signals indicating each bit value from one another, and generating the second modulated signal using the second modulation technique by generating signals having different lengths for each at least two-bit values of coded address data.

55. The computer readable storage medium of claim 51, wherein the generation of the first modulated signal comprises generating at least two pattern signals indicating at least two-bit values of the coded address data using the first modulation technique, and generating the second modulated signal using the first modulation technique by generating at least two signals used to distinguish signals indicating a bit value of the address data using the second modulation technique, where the coded address data of at least two bits is indicated by disposing at least two pattern signals in predetermined locations and inserting the at least two signals to distinguish signals indicating a bit value of the address data between the at least two pattern signals.

56. The computer readable storage medium of claim 52, wherein the generation of the unit wobble signal comprises disposing the first and second modulated signals adjacent to each other.

57. The computer readable storage medium of claim 52, wherein the generation of the unit wobble signal comprises alternating the first and second modulated signals.

58. The computer readable storage medium of claim 54, further comprising:

generating signals indicating each bit of the coded address data.

59. A computer readable recording medium to demodulate address data of a disc type recording medium, comprising:

a demodulating unit, after receiving a unit wobble signal indicating the address data of at least two bits generated by synthesizing signals modulated by first and second modulation techniques, demodulating, using the first demodulation technique, the signal modulated by using the first modulation technique into data of the at least two bits, and demodulating, using the second demodulation technique, the signal modulated by using the second modulation technique into data of the at least two bits;

a data determining unit determining the address data based on the data demodulated by using the first and second demodulation techniques and generates an eraser flag signal indicating mismatched bit positions if values of the data demodulated by using the first and second demodulation techniques are different from each other; and

an error correction decoding unit performing error correction decoding of the determined address data and the eraser flag signal.

60. The computer readable recording medium of claim 59, the demodulating unit comprises:

a first demodulator demodulating the data using the first demodulation technique; and

a second demodulator demodulating the data using the second demodulation technique.

61. The computer readable recording medium of claim 59, wherein the demodulating unit comprises:

a first demodulator demodulating, using the first demodulation technique, the signal modulated by using the first modulation technique into a first bit value of the address data, if a predetermined pattern signal exists, and demodulating, using the first demodulation technique, the signal modulated by using the first modulation technique into a second bit value of the address data if the predetermined pattern signal does not exist; and

a second demodulator demodulating using the second demodulation technique each bit value of the signal modulated by using the second modulation technique.

62. The apparatus of claim 37, wherein the BPSK and FSK pattern signals alternate in the unit wobble signal.

63. The apparatus of claim 37, wherein the start of the address data of the at least two bits is indicated by using BPSK signals indicating the bit value "0" or "1" of the address data of the at least two bits.